



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,079	03/30/2001	Errol C. Heiman	STL9524	6981

27365 7590 05/16/2008
SEAGATE TECHNOLOGY LLC C/O WESTMAN
CHAMPLIN & KELLY, P.A.
SUITE 1400
900 SECOND AVENUE SOUTH
MINNEAPOLIS, MN 55402-3244

EXAMINER

LEROUX, ETIENNE PIERRE

ART UNIT	PAPER NUMBER
----------	--------------

2161

MAIL DATE	DELIVERY MODE
-----------	---------------

05/16/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/823,079	Applicant(s) HEIMAN ET AL.	
	Examiner Etienne P. LeRoux	Art Unit 2161	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 March 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18-21,23-31 and 33-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 18-21,23-31 and 33-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Prosecution Reopened

In view of the Appeal Brief filed on 3/11/2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Apu M Mofiz/

Supervisory Patent Examiner, Art Unit 2161

Claim Status:

Claims 18-21, 23-31 and 33-36 are pending; claims 1-17, 22, 32 and 37 have been canceled. Claims 18-21, 23-31 and 33-36 are rejected as detailed below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 18-20, 24-30 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pat No 5,712,553 (Hallberg) in view of US Pat No 5,970,074 issued to Ehiro (hereafter Ehiro).

Claims 18 and 28:

Hallberg discloses:

a multi-voltage power source having a first voltage output, which is capable of supplying a plurality of selectable voltage levels

[col 2, lines 55-63,

The present invention also provides a method for supplying at least two different voltages from a power supply having a plurality of batteries, including a first voltage from substantially all the batteries. The method comprises the steps of providing at least a second voltage from at least one battery, the second voltage being equal to a proportional fraction of the first voltage]

for a constant power supply voltage at a nominal power supply voltage of an electronic device

[col 1, lines 13-15,

Portable electronic devices sometimes require multiple voltages for operation]

an additional power source having a second voltage output, which is capable of supplying an additional voltage level that is different from the plurality of selectable voltage levels

Art Unit: 2161

[col 10, line 66 through col 11, line 12]

In an alternative embodiment of the present invention, a first group of at least three batteries, or voltage subgroups is operatively connected to supply a first voltage, the power supply also providing at least a second and third voltage supplied from subgroups of the first group that includes at least one battery, the second and third voltages being less than the first voltage]

Hallberg discloses the elements of the claimed invention as noted above but does not disclose circuitry configured to introduce controllable disturbances into the constant power supply voltage. Ehiro discloses circuitry configured to introduce controllable disturbances into the constant power supply voltage [Figs 1, 4 and 5, col 7, lines 10-50]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hallberg to include circuitry configured to introduce controllable disturbances into the constant power supply voltage as taught by Ehiro for the purpose of measuring the threshold characteristic of a semiconductor integrated circuit [col 2, lines 15-20].

Claims 19 and 29:

The combination of Hallberg and Ehiro discloses the elements of the claimed invention as noted above and further Ehiro discloses wherein the disturbance is a rising pulse having a maximum voltage which is controllable [Fig 4, col 7, lines 10-20, alternatively, Test Step in Fig 5 can be interpreted as comprising a negative step pulse and a positive step pulse]

Claims 20 and 30:

The combination of Hallberg and Ehiro discloses the elements of the claimed invention as noted above and further Ehiro discloses wherein the disturbance is a low-going pulse having a minimum voltage being less than the nominal power supply voltage [Fig 5]

Claims 24 and 34:

Art Unit: 2161

The combination of Hallberg and Ehiro discloses the elements of the claimed invention as noted above and further Ehiro discloses a manually operated user interface used to control the disturbances [col 6, lines 35-45]

Claims 25 and 36:

The combination of Hallberg and Ehiro discloses the elements of the claimed invention as noted above and further Ehiro discloses wherein the disturbance is a plurality of pulses and a frequency and a number of pulses in the plurality of pulses are controllable [, col 6, lines 35-45, Fig 5]

Claim 26 and 35:

The combination of Hallberg and Ehiro discloses the elements of the claimed invention as noted above and further Ehiro discloses wherein the disturbance is at least one pulse having a duration and a magnitude which are controllable [Fig 5]

Claim 27:

The combination of Hallberg and Ehiro discloses the elements of the claimed invention as noted above and further Ehiro discloses wherein the disturbance comprises a voltage sequence applied during powering up of the electronic device [Fig 5]

Claims 21 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hallberg and Ehiro and further in view of US Pat No 5,386,183 (Cronvich), hereafter Cronvich.

Claim 21 and 31:

Art Unit: 2161

The combination of Hallberg and Ehiro discloses the elements of claims 18/28 as noted above but does not disclose wherein the constant power supply voltage is selected from the group of voltages consisting of +5 VDC and +12 VDC. Cronvich discloses wherein the constant power supply voltage is selected from the group of voltages consisting of +5 VDC and +12 VDC [Fig 3 and col 12, lines 23-26]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify then above combination of references to include wherein the constant power supply voltage is selected from the group of voltages consisting of +5 VDC and +12 VDC as taught by Cronvich for the purpose of providing a power source suitable for many microcomputer and logic circuits [col 12, lines 23-26].

Claims 23 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hallberg and Ehiro and further in view of US Pat No 4,764,652 (Lee et al), hereafter Lee.

Claims 23 and 33:

The combination of Hallberg and Ehiro discloses the elements of claims 18 and 22/ 28 and 32 as noted above but does not disclose wherein the additional voltage is +24VDC. Lee discloses +24VDC [col 1, lines 55-60]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above combination of references to include wherein the additional voltage is +24VDC as taught by Lee for the purpose of including a power supply voltage that is used for telecommunications equipment [col 1, lines 55-60].

Response to Arguments

Art Unit: 2161

Applicant's arguments filed 3/11/2008 have been carefully considered but are not persuasive for the following reasons.

Applicant Argues:

Applicant argues that the combination of Hallberg and Ehiro does not disclose the claim 1 limitation “circuitry configured to introduce disturbances into the constant power supply voltage.”

Examiner Responds:

Examiner is not persuaded. Ehiro in Figure 3 discloses $V_{DD} = 5.00V$. Furthermore, Ehiro discloses in column 6, lines 55-60 that $V_{DD} = 5 V$ is the supply voltage.

Furthermore, V_{DD} is well-known in the art as the nomenclature for indicating a power supply voltage. Furthermore, 5 Volts is a well-known power supply voltage for integrated circuits. In support of examiner's assertion that the above is well-known, examiner provides additional reference US Pat No 6,013,386 (Cole, et al). Cole's disclosure in the abstract, Figure 2b, and column 9, lines 55-60 is pertinent.

Contact Information

Art Unit: 2161

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Etienne P. LeRoux whose telephone number is (571) 272-4022.

The examiner can normally be reached on Monday through Friday, 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Apu Mofiz can be reached on (571) 272-4080. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

5/12/2008

/E. P. L./

Primary Examiner, Art Unit 2161

/Apu M Mofiz/

Supervisory Patent Examiner, Art Unit 2161